



Citation	M. Strackx, E. D'Agostino, P. Leroux and P. Reynaert, 2015, Direct RF Subsampling Receivers for Breast Cancer Detection with Impulse-Based UWB Signals IEEE Transactions on Circuits and Systems-II, vol. 62, no. 2, pp.144-148.
Archived version	Author manuscript: the content is identical to the content of the published paper, but without the final typesetting by the publisher
Published version	http://dx.doi.org/10.1109/TCSII.2014.2387676
Journal homepage	http://ieee-cas.org/
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Direct RF Subsampling Receivers for Breast Cancer Detection with Impulse-Based UWB Signals

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Abstract—The implementation of a Direct RF Subsampling Receiver in CMOS is presented for the application of breast cancer detection using impulse based ultra-wideband (UWB) signals. Such a receiver inherently benefits from CMOS scaling since its speed-accuracy trade-off depends only on technological process parameters. With a proper choice of antenna matching media, the current signal processing requested resolution can be translated into feasible hardware specifications. The track and hold (T/H) circuit is analyzed and implemented in a 40 nm chip since this block must cope with the full RF bandwidth. An Effective Resolution Bandwidth (ERBW) of 5.5 GHz was measured with an accuracy of 6-b for rail-to-rail input signals. Secondly, a 2-stage Miller compensated Fully Differential Difference Amplifier (FDDA) is discussed with low input parasitics (10 fF) to enable measurements without limiting the performance.

Index Terms—track and hold, ultra-wideband (UWB) receiver, CMOS integrated circuits.

I. INTRODUCTION

MAMMOGRAPHY is currently the most frequently used method for breast cancer screening. However, false positive results are likely to occur. Up to 24% of examined women during a 10 year period got at least one false positive diagnosis [1]. Moreover, the use of ionizing radiation, such as X-rays, may also have a cancer inducing effect on the long term, and should therefore be minimized [2]. Microwave imaging is considered to be a viable alternative compared to existing mammography and MRI (Magnetic Resonance Imaging) [3] techniques. Current microwave imaging demonstrators use commercial VNAs (Vector Network Analyzer) [4]. CMOS solutions, based on SFCW (Stepped Frequency Continuous Waveforms) are also reported, where a single frequency tone is swept over time [5]. A different approach describes the usage of impulse based ultra-wideband (UWB) signals with confocal imaging [2] or time reversal [6] algorithms. However, hardware in CMOS is still lacking due to both high bandwidth and high resolution requirements [7]. Still, RF sampling architectures can benefit from CMOS scaling [8]. Another advantage is the fact that the sampler can operate rail-to-rail

This work was supported by the Belgian Nuclear Research Centre SCK-CEN.

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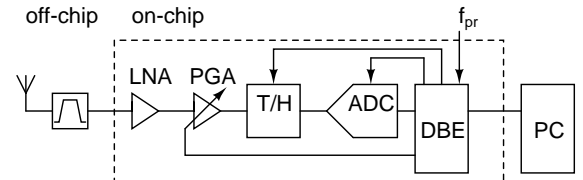


Fig. 1. Direct RF subsampling receiver block diagram.

thereby achieving maximum SNR for a given kT/C noise floor if the bootstrapping technique is used.

To cope with reliability issues caused by the introduction of bootstrapping, the following techniques were introduced: non-overlapping clocks, bulk switching and hold capacitor precharging [9]. The previous work is extended by broad analysis here. First, Section II, analyzes the required receiver dynamic range (DR) for a targeted breast cancer detection application without any signal processing gain. In order to lower the required DR, this work proposes to use H_2O as antenna matching media. Section III then analyzes the bandwidth resolution trade-off of the bootstrapped T/H circuit and elaborates on an additional over-voltage issue of the classical bootstrapping circuit. It is proven that the proposed receiver inherently benefits from CMOS scaling. To allow measurements of the T/H without compromising its inherent bandwidth, a fully differential output buffer is described. It has both low input parasitics (10 fF) to maintain high RF input bandwidth and yet achieve 50 Ohm driving capability. Section IV contains the measured performance of the T/H. Measurement results of [9] are extended by analyzing resolution as a function of input power and frequency. Due to bootstrapping, the T/H is capable of maintaining the resolution from -15 dBm to 7 dBm of input power.

II. RECEIVER SYSTEM LEVEL

The block diagram of the considered direct RF subsampling receiver is shown in Fig. 1. The incoming UWB pulse is first filtered by the antenna itself or off-chip components before entering the low-noise amplifier on-chip. Then a programmable gain amplifier (PGA) provides optimal mapping of the input signal to the full ADC and T/H input range. The receiver digital back end (DBE) receives the pulse transmission rate f_{pr} from the transmitter and generates the desired subsampling frequency. The period of the sampling clock in this design has a 4 ps time offset compared to the pulse transmission period.

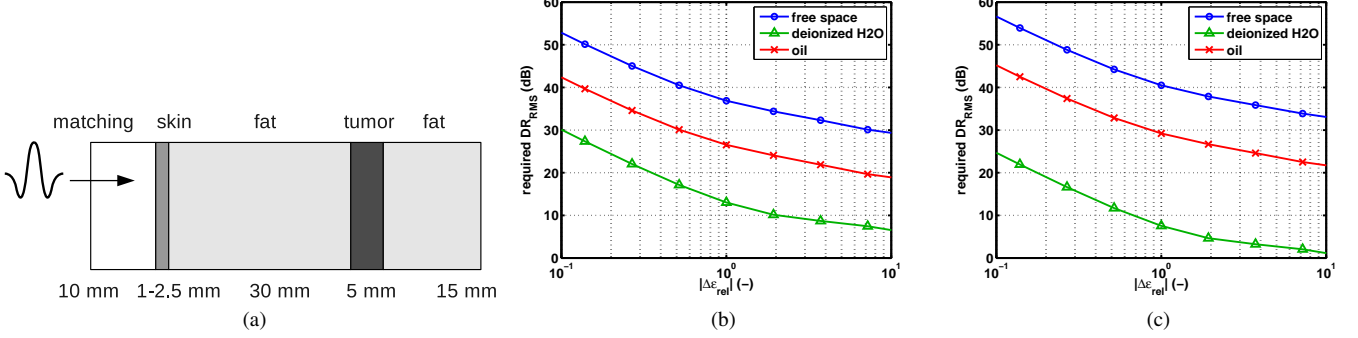


Fig. 2. 1D cross section of the breast phantom (a) and simulated DR as a function of dielectric contrast with 1 mm (b) and 2.5 mm (c) skin.

A. Receiver dynamic range calculation

For wideband receivers, the bandwidth-accuracy trade-off is the key performance factor. In order to have circuit resolution specifications yet make abstraction of any image processing algorithm, a 1D signal path model is used to predict the necessary receiver dynamic range (DR) for a given difference in dielectric contrast of the tumor. An important issue to ease the receiver DR is the initial matching media-skin interface. Previously, different kinds of coupling media were utilized not only for the design and measurements of antennas but also for signal processing evaluation of the whole setup. Antennas are mostly designed to radiate in oil with a $\epsilon_r = 10$ [10]. In this case, the medium matches to the underlying fat layer of the breast. On the other hand deionized (DI) water is used in [11] as coupling medium to minimize heat generation in the human skin during hyperthermia treatment of breast cancer.

To analyze the relative influence of different coupling media, a 1D electromagnetic (EM) model of the signal path was built and validated using linear transmission line theory [12]. For a basic understanding of the model, the reader is also referred to [13]. Fig. 2a depicts the layered setup of the model along with the dimensions. The structure is placed in the far field and couples to the antennas by a matching medium. It also makes abstraction of any signal processing algorithm. This is necessary because the final performance is limited by the analog-to-digital converter (ADC) dynamic range (DR) of the receiver. The limitation is created in hardware before any digital signal processing can aid. Sensitivities depending on tumor size, depth and dielectric contrast are ranging from 50 dB (8 bit) [7], 80 dB (13 bit) [3] up to 100 dB (16 bit) [5], the latter for a setup with the antennas located in free-space. This requirement can be severely relaxed by proper choice of an antenna matching medium, hence allowing RF sampling. According to current state-of-the-art ADCs [14], a DR of 40 dB could be achieved using a bandwidth of 10 GHz and assuming a jitter specification on the sampling clock of $\sigma_{rms} = 100fs$. This gap can however be minimized. Considering Fig. 2a, for different coupling media, there is a tumor layer included of which the complex permittivity is changed relatively to the surrounding averaged fat value. According to [15] the dielectric contrast ranges from 10 % to a factor of 10. A single pole Debye model is used for complex permittivity fitting, specific values can be found in [11]. The

model itself calculates the global reflection coefficient of the multilayered structure. However, this function provides little practical insight. The function can be further used to calculate the reflected UWB pulse for a given excitation. Therefore we apply a gaussian doublet as

$$g(t) = \frac{1 - (t - b)^2}{\sigma^2} e^{-\frac{(t-b)^2}{2\sigma^2}} \quad (1)$$

Where σ is chosen 41 ps to fit the spectral FCC mask and b is an arbitrary time shift to avoid negative values on the time axis. We can derive the DR value as

$$DR_{RMS} = 20 \log_{10} \frac{[g_0(t)]_{RMS}}{[g_{\Delta}(t) - g_0(t)]_{RMS}} \quad (2)$$

Where $g_0(t)$ is the initial reflected pulse without any tumor layer. The reflected pulse $g_{\Delta}(t)$ occurs when a change in complex permittivity is present in the tumor layer. It is the difference between both cases that determines the minimum change which needs to be detectable. This difference is compared relatively to the initial reflection. Intuitively, it is more difficult to detect the same difference when the initial matching-skin reflection is higher, hence setting the upper signal level and requiring a larger DR of the ADC.

The required DR for different coupling media with a skin layer of 1 mm thickness and 2.5 mm is shown in Fig. 2b and Fig. 2c respectively. For a 1 mm skin layer, the difference in DR for free space and skin coupling media is 26 dB. If the skin thickness is increased to 2.5 mm, the difference is 31 dB. This illustrates the importance of choosing a correct matching medium or even radiating directly into the human body. The DR requirement can be roughly halved as indicated in Fig. 2c. From a hardware point of view it is important to reduce the initial large skin reflection, avoiding saturation of the receiver.

III. RECEIVER CIRCUIT DESIGN

In order to relax the ADC requirements in terms of speed or throughput, the subsampling technique can be used, however, at the cost of noise folding. Here, the signals are sampled at a rate slightly different from the pulse repetition rate. The sampler inherently down-converts the input signal. Such architecture can also be referred to as an RF sampling receiver [8]. However, the T/H must still cope with the full signal bandwidth and hence faces the same speed-accuracy trade-off as

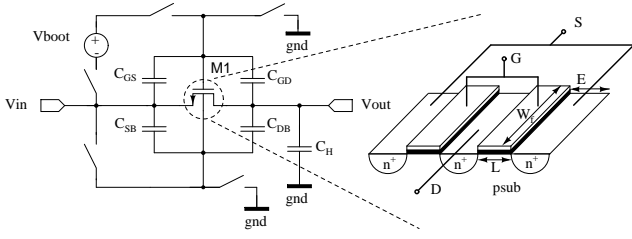


Fig. 3. Single ended T/H circuit representation with RF switch parasitics.

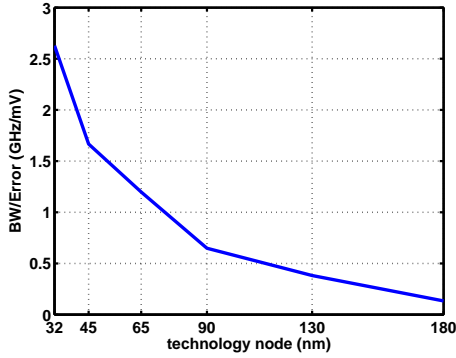


Fig. 4. BW/Error ratio scaling with technology nodes caused by signal dependent clock feedthrough.

Nyquist samplers. Consider the circuit of Fig. 3 as single ended representation of a differential T/H. In order to achieve high bandwidth and allow CMOS scaling, the bootstrapping circuit is used to operate rail-to-rail in nanometer CMOS technology nodes as it provides an input independent switch on-resistance. However, this advantage comes at the cost of signal dependent clock feedthrough and the risk of over-voltage issues. For the latter reason, the bulk of $M1$ is modulated between V_{in} during the track-phase and V_{ss} during the hold-phase [9].

A. T/H design methodology and CMOS scaling

In order to achieve high bandwidth, as indicated by equation 3 [16], the switch transistor should have high overdrive voltage and low parasitic drain capacitance. Therefore an even number of fingers is preferred to reduce the amount of drain junctions. The even amount of transistor fingers N , only has influence on the sidewall capacitance C_{jsw} , as indicated by equations 4. Where $W = W_f N$ is the total transistor width and E is the junction length. Typically in the triode region, C_{GD} is one order larger than C_{DB} , leaving neglectable influence of N .

$$f_{-3dB} = \frac{K_n \frac{W}{L} (V_{GS} - V_{th0})}{2\pi(C_H + C_{dd})} \quad (3)$$

$$C_{GD} = WC_{ov} + \frac{WLC_{ox}}{2} \quad (4a)$$

$$C_{DB} = \frac{W}{2} EC_j + (W + EN)C_{jsw} \quad (4b)$$

For a kT/C sized hold capacitor and a desired BW, an upper resolution limit is set, shown in equation 5. Due to

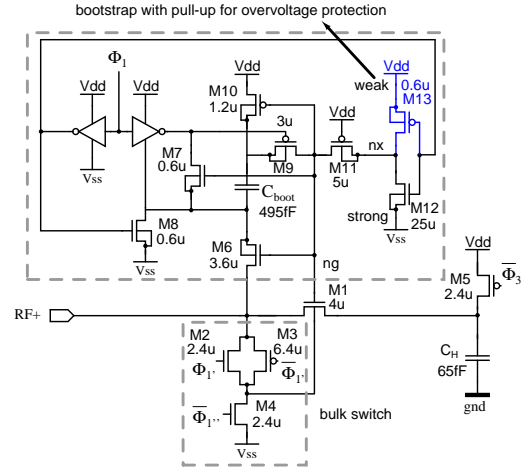


Fig. 5. T/H circuit with bootstrap, bulk switch and precharge switch.

bootstrapping and bulk switching the total error is written as $\Delta V_{err} = \Delta V_{CLK} + \Delta V_{BS}$ with each error source derived according to equations 6. Using a differential T/H causes the V_{DD} part of equation 6(a) to appear as a common-mode and signal independent offset.

$$N = \frac{\log(\frac{\Delta V_{in}}{\Delta V_{error}})}{\log(2)} = \frac{\log\left(\frac{C_H}{W} \frac{1}{C_{ov} + \frac{LC_{ox}}{2} + \frac{EC_j}{2} + C_{jsw}}\right)}{\log(2)} \quad (5)$$

$$\Delta V_{CLK} = (V_{DD} + V_{in}) \frac{C_{GD}}{C_{GD} + C_H} \approx (V_{DD} + V_{in}) \frac{C_{GD}}{C_H} \quad (6a)$$

$$\Delta V_{BS} = V_{in} \frac{C_{DB}}{C_{DB} + C_H} \approx V_{in} \frac{C_{DB}}{C_H} \quad (6b)$$

This raises the question if and how the bandwidth-error ratio can be maximized. Neglecting the bulk modulation here and assuming the gate oxide capacitance is dominant, equation 7 is proposed. If the bootstrap voltage is set at V_{DD} along with a rail-to-rail input signal, the ratio is only dependent on technology parameters providing an upper design limit. In other words for a targeted bandwidth, the error is unaffected by the switch width W or hold capacitor C_H . Based on predictive technology models [17] and equation 7, Fig. 4 is calculated. As shown, even due to the reduced supply voltage, scaling continues as the gate length's influence is quadratic.

$$\frac{BW}{\Delta V_{err}} = \frac{\mu_n (V_{GS} - V_{th0})}{2\pi V_{in} L^2} = \frac{\mu_n}{2\pi L^2} \left(1 - \frac{V_{th0}}{V_{DD}}\right) \quad (7)$$

B. T/H with bootstrap and bulk switch circuits

Bootstrapping a rail-to-rail input T/H can not only raise over-voltages in the switch but also in the bootstrapping circuit itself. Consider the $M1$ gate pull-down path from Fig. 5. For a short fall time, $W_{M12} = 5W_{M11}$ was simulated, leading to an asymmetric voltage division in the classical bootstrapping circuit at the high impedant node nx . If a minimum sized PMOS transistor $M13$ is added, node nx can be pulled to V_{dd} during the tracking-phase. Fig. 6 shows the voltages at nodes ng and nx at source and drain of $M11$ for a 1 GHz RF

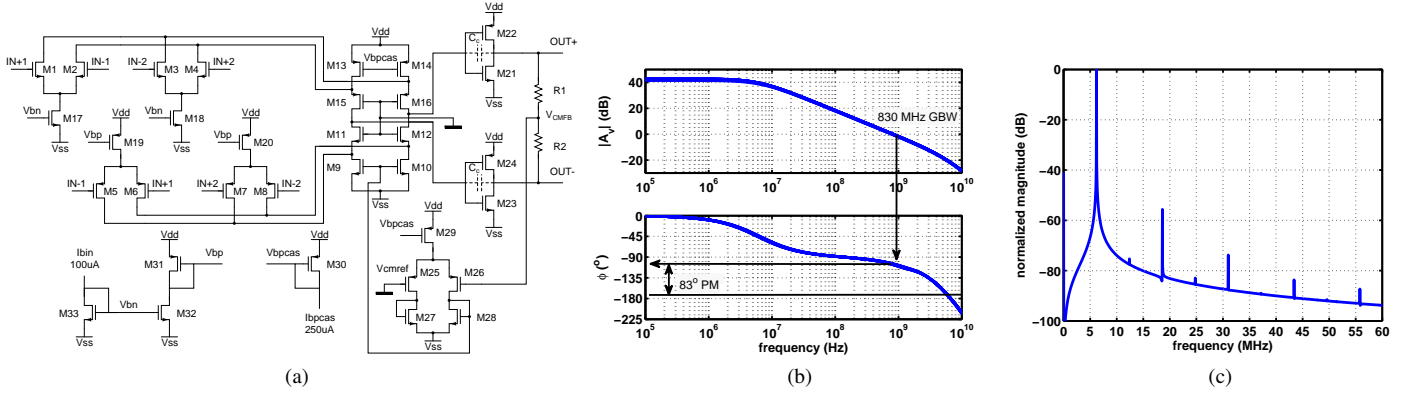


Fig. 7. 2-stage Miller compensated folded cascode FDDA output buffer with CMFB and a class-AB push-pull second stage for high linearity (a), Post lay-out simulated FDDA gain and phase response during a 0.9 V DC input bias sweep (b), Post lay-out simulated FDDA linearity at $f_{in} = 6.2$ MHz with an SNDR of 55 dB (c).

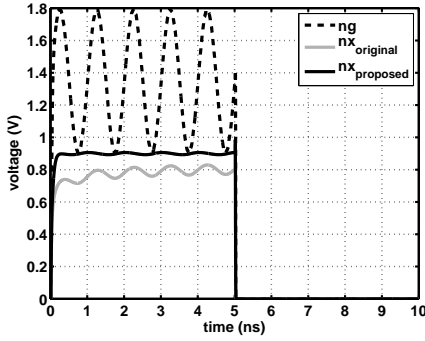


Fig. 6. Effect of pull-up transistor M13 avoiding reliability issues between source and drain of transistor M11 in the bootstrap circuit.

input. The latter frequency is chosen for displaying purposes. The bulk switch is designed as a transmission gate along with a discharge NMOS switch in order to ground the bulk of $M1$ during the hold-phase. The sizing of the transmission gate faces a trade-off between the bulk-source effect and isolation during the hold-state. In this case, transistors $M2, M4$ were designed minimum sized and $W_{M3} \approx 2.5W_{M2}$ in order to keep parasitics small. Precharge switch $M5$ is also minimum sized for the same reason. A detailed description of the differential RF core and its multi-phase clocking scheme is covered in [9].

C. High linearity output buffer with low input capacitance

The unity gain buffer is implemented with a unity feedback opamp and consist of two stages: a pre-amplifier with a low input capacitance of 9.3 fF and a high linearity miller compensated class-AB 50Ω driver, as shown in Fig. 7a. The corresponding device dimensions are listed in Table I. Complementary input pairs are used in the 2.5 V output buffer in order to operate across the 0.9 V input rail. Due to symmetrical power supplies, there is no need for voltage translation or input biasing. The fully differential difference amplifier [18] technique was applied to a folded cascode structure. C_{GD} of the second stage acts as Miller compensation. Unity gain feedback provides the bias point of the second stage. Common mode feedback (CMFB) is then realized using

TABLE I
FDDA OUTPUT BUFFER DEVICE DIMENSIONS.

W_{M1-8}	W_{M32-33}	W_{M17-18}	W_{M31}	W_{M19-20}	W_{M30}
4 μ	5 μ	10 μ	20 μ	40 μ	10.5 μ
W_{M13-14}	W_{M15-16}	W_{M11-12}	W_{M9-10}	$W_{M22,24}$	$W_{M21,23}$
42 μ	95 μ	50 μ	24 μ	150 μ	100 μ
W_{M29}	W_{M25-26}	W_{M27-28}	R_{1-2}	C_c	L
42 μ	36 μ	12 μ	400 Ω	160 fF	270 nm

resistive sensing. Since the output impedance is 50Ω , low valued sensing resistors $R1, R2$ of 400 Ω do not compromise the CMFB phase margin. The open loop gain of the opamp determines the SNDR/ENOB and was designed here for 40 dB. The targeted 3-dB cut-off frequency is set by the maximum RF input signal frequency f_{RF} , equivalent time (ET) offset t_{eq} and sample frequency f_s or UWB pulse repetition rate f_{pr} . A small ET offset is desired for accurate signal reconstruction, typically 4 ps here. Together with a 10 GHz RF input and a sample frequency of 100 MHz, this results in an output frequency of 4 MHz using equation 8.

$$N_{points} = \frac{T_{RF}}{t_{eq}} \quad f_{out(ET)} = \frac{f_{pr}}{N_{points}} \quad (8)$$

Simulations show an open-loop gain of 42.5 dB with a variation of only ± 0.66 dB across the full input range with a phase margin of $83^\circ \pm 0.7^\circ$. A bandwidth of 6.2 MHz ± 0.36 MHz is achieved. The open loop gain and phase responses are shown in Fig. 7b for changing DC input bias. The resulting GBW of the amplifier is 830 MHz ± 35 MHz. Fig. 7c shows the linearity of the output buffer at the 3-dB cut-off frequency of 6.2 MHz. An SNDR of 55 dB is achieved, corresponding to 8.8 bits, higher than the inherent T/H sampling linearity.

IV. MEASUREMENT RESULTS

The T/H circuit and output buffer are implemented in 40 nm CMOS. Fig. 8 provides a detailed microphotograph of the RF core. The RF switch, hold capacitors and RF feedthrough cancellation paths are surrounded by dummies for matching purposes. The bulk switch is located next to the RF switch to reduce parasitics. Dummy metals are blocked under the critical

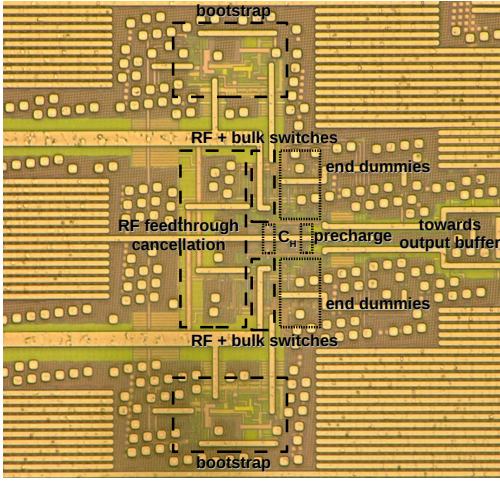


Fig. 8. Microphotograph of the T/H core with bootstrap circuit, bulk & precharge switches and RF feedthrough cancellation.

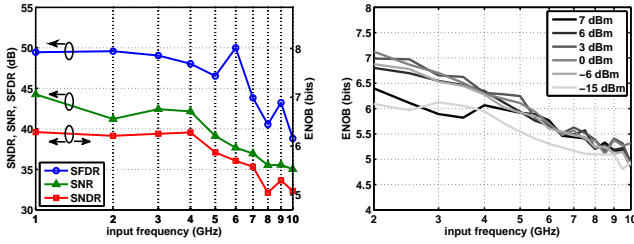


Fig. 9. Measured SNDR (ENOB), SNR and SFDR for a 7 dBm rail-to-rail input signal achieving 6.3 bit up to 4 GHz (left) and ENOB in the 2-10 GHz range for an input power sweep from -15 dBm to 7 dBm reaching a max resolution of 7.1 bit (right).

RF traces. Fig. 9 depicts the measured resolution for a 7 dBm rail-to-rail input signal taking losses of the measurement setup into account. A resolution of 6.3-b was measured with a corresponding effective resolution bandwidth of 5.5 GHz while consuming 1.4 mW for the core circuits. Comparing this result with the rail-to-rail analysis of section III, based on predictive models, a resolution of 6.6-b is expected for a 5.5 GHz bandwidth as first order estimate. Previously, the circuit was measured using UWB gaussian pulses [9], maintaining a pulse fidelity of 99.5 %. In order to analyze the application for pulse based UWB signals further, the circuit performance was measured for a sweep of input power. The input power was swept from -15 dBm up to 7 dBm, as shown in Fig. 9. The advantage of bootstrapping is clear here, since the ENOB is maintained for high input power, whereas in the classical approach, the resolution would drop for much smaller power levels in nanometer CMOS. Pulse based signals with high peak-to-average power ratios (PAPR) can be digitized with the same resolution order. At 7 dBm input, saturation can also be noticed, at -15 dBm the influence of noise becomes more important. For smaller input signals, clock jitter which is in the order of $400 - 450 f_{s_{rms}}$ is the dominant error source causing the -20 dB per decade drop.

V. CONCLUSION

This brief presents a direct RF subsampling receiver for breast cancer detection using impulse based UWB signals.

It is proven that the T/H in combination with bootstrapping inherently benefits from CMOS scaling and is capable of maintaining performance for UWB pulses with high PAPR. As shown by the 1D EM model, antenna matching is important at the system level to lower the required DR and enable CMOS implementations. A 40 nm T/H chip is presented, capable of achieving 6-b resolution with an ERBW of 5.5 GHz for rail-to-rail input signals. A resolution higher than 6-b is maintained from -15 dBm to 7 dBm. In order to have both high RF bandwidth and linear 50Ω driving capability a cascode based FDDA with complementary input pairs is proposed.

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